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ABSTRACT

The present invention relates to a non volatile memory device architecture, for example of the Flash type, incorporating a memory cell array and an input/output interface to receive memory data and/or addresses from and to the outside of the device. The interface operates generally according to a serial communication protocol, but it is equipped with a further pseudo-parallel communication portion with a low pin number incorporating circuit blocks for selecting the one or the other communication mode against an input-received selection signal.